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Abstract: In real-time systems, the use of hardware accelerators can lead to a worst-case execution-time speed-up, to a simplification of its analysis, and to a reduction of its pessimism. When using FPGA technology, dynamic partial reconfiguration (DPR) can be used to minimize the area, by only loading those accelerators that are needed at any given point in time.

A Controller for Dynamic Partial Reconfiguration in FPGA ...

The dynamic partial reconfiguration (DPR) feature offered by modern FPGAs can be used to overcome this limitation, by enabling run-time reconfiguration of selected regions on the FPGA. This allows a more efficient utilization of FPGA resources since HwAs that are only required for limited amounts of time can be replaced when the functionality implemented in these regions is no longer required.

Using dynamic partial reconfiguration of FPGAs in real ...

Dynamic reconfiguration enables hardware adaptation even during run-time. This paper concentrates on extending the application of dynamically reconfigurable logic to the area of network interface logic.

Dynamic Reconfiguration of Real-Time Network Interfaces - CORE

In real-time systems, the use of hardware accelerators can lead to a worst-case execution-time speed-up, to a simplification of its analysis, and to a reduction of its pessimism. When using FPGA technology, dynamic partial reconfiguration (DPR) can be used to minimize the area, by only loading those accelerators that are needed at any given point in time.

A Controller for Dynamic Partial Reconfiguration in FPGA ...

Dynamic Reconfiguration. Real-time code generated for a model is managed on the target by a management system called the QUARC Target Manager. It is the QUARC Target Manager that allows generated real-time code to be seamlessly downloaded and run on the target from Simulink. One of the advanced features of this management system is the support for dynamic reconfiguration.

Dynamic Reconfiguration :: QUARC

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