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Available in the Cadence®Tempus™Timing Signoff Solution, scope-based timing analysis lets you dynamically abstract only those portions of the design that you want to analyze. And, you can analyze the portion with full chip-level context.

Techniques to Accelerate Power and Timing ... - Cadence

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The Cadence Design Communities support Cadence users and technologists interacting to exchange ideas, news, technical information, and best practices to solve problems and get the most from Cadence technology. The community is open to everyone, and to provide the most value, we require participants to follow our Community Guidelines that facilitate a quality exchange of ideas and information ...

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Length : 2 days Digital Badge Available This course is a detailed exploration of the Tempus™ Timing Signoff Solution, which supports distributed processing and enables fast static timing analysis with full signal integrity (SI) and glitch analysis, statistical variation (SOCV), and Multi-Mode and Multi-Corner (MMMC) analysis. In this course, you analyze a design for static timing and signal ...

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A new common user interface that the Genus synthesis solution shares with Cadence Innovus ™ Implementation System and Cadence Tempus ™ Timing Signoff Solution streamlines flow development and simplifies usability across the complete Cadence digital flow.

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The Tempus Power Integrity Solution integrates the widely used Cadence Tempus Timing Signoff Solution and the Voltus IC Power Integrity Solution. Customers using the new tool will be able to significantly lower IR drop design margins without compromising signoff quality, improving power and area. Early use cases have shown that Tempus correctly identified IR drop errors, avoiding silicon ...

Cadence announces the Tempus Power Integrity Solution

As part of the collaboration, the Cadence ® digital, signoff and custom/analog tools have been certified for Design Rule Manual (DRM) and SPICE v1.0, and Cadence IP has been enabled for the TSMC 5nm process.